REMARKS/ARGUMENTS

Claim rejections 35 USC § 102

Claims 1-28 were rejected, under 35 USC 102(b), as being allegedly anticipated by Profit, Jr. U.S. Pat. No. 5,911,059 (hereinafter, Profit). The Applicant respectfully traverses the rejection.

As per Claims 1-28:

Independent Claim 1 recites a limitation whereby the device under test operates in lock-step fashion with the emulator device, as claimed. Moreover, independent Claim 1 recites a limitation whereby a first signal is received, initiating the sleep function at the device under test, and one or more clock of the device under test are turned off, as claimed. Independent Claim 1 further recites a limitation whereby the emulator device discontinues execution of instructions in lock-step upon turning off the clock, as claimed.

Profit discloses that part of the target hardware is modeled by the processor emulator 202 and part of it is modeled by a hardware simulator 210 running on the host computer 214 (see Profit, col. 5, lines 62-65). As such, the Applicant understands Profit to teach that the target hardware is modeled by the combination of the processor emulator 202 and the hardware simulator 210. Profit further discloses that a controller within a communication interface sets the

CYPR-CD01208M US App. No.: 09/989,777 Art Unit: 2123 Examiner: Sharon, Ayal I residing on the processor emulator 202 to be synchronized with the simulation circuitry in the hardware simulator 210 (see Profit, col. 11, lines 27-43). As such, the Applicant understands Profit to teach synchronization between the processor emulator 202 and the hardware simulator 210 wherein the target hardware is modeled. As such, Profit neither teaches nor suggests the recited limitation of independent Claim 1 because Profit teaches synchronization between different emulator components (processor emulator 202 and hardware simulator 210) that model the target hardware whereas independent Claim 1 recites lockstep operation between the device under test and the emulator device, as claimed.

Moreover, "a claim is anticipated <u>only if each and every element</u> as set forth in the claim is found, <u>either expressly or inherently</u> described, in a single prior art reference." Verdegaal Bros v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The rejection asserts that "because part of the target hardware (the "device under test") is modeled by the processor emulator, and part is modeled by the hardware simulator running on the host computer, the processor emulator operates in lockstep with the portion of the "device under test" running in the software simulator." The Applicant respectfully disagrees because modeling the processor emulator based on the hardware simulator and the processor emulator <u>does not necessarily</u> imply that the combination of hardware simulator and the processor emulator operates in <u>lock</u>

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step with the "device under test." As such, Profit fails to expressly or inherently disclose the device under test operating in lock-step with the emulator device, as claimed.

Furthermore, the Applicant agrees with the rejection asserting that Profit teaches that the controller halts the emulator's processor (see Profit, col. 9 line 40 to col. 10, line 31). The Applicant respectfully directs the Examiner's attention to the fact that held to col. 10, line 31). The Applicant respectfully directs the Examiner's attention to the fact that held to col. 10, line 31). The Applicant respectfully directs the Examiner's attention to the fact that held to col. 10, line 31). The Applicant respectfully directs the Examiner's attention to the fact that held to col. 10, line 31). The Applicant respectfully directs the Examiner's attention to the fact that held to col. 10, line 31). The Applicant respectfully directs the Example.

Moreover, Profit discloses that "upon receiving the clock synchronization acknowledge signal, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22" (see Profit, col. 12, lines 24-35). Accordingly, Profit only discloses that execution of the target program 22 continues when the controller 228 activates the RESET signal. As such, Profit fails to expressly or inherently disclose that the emulator device discontinues execution of instructions in lock-step upon turning off the clock, as claimed. Additionally, the rejection asserts that "since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal turned off the clock, as claimed by the applicant." The Applicant respectfully disagrees. The clock synchronization activates the RESET signal which releases the RUN/HALT

Art Unit: 2123 Examiner: Sharon, Aval I signal. As such, it is not the RUN/HALT signal reactivating the clock as asserted by the rejection but it is the clock synchronization activating the RESET signal causing the RUN/HALT signal to be released. Therefore, it is not inherent that the initial RUN/HALT signal turned off the clock. In fact Profit teaches away from turning off the clock because in order to receive clock synchronization, the clock must necessarily be on.

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' "In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As such the Applicants respectfully invite the Examiner to introduce extrinsic evidence to establish the alleged inherency or to kindly withdraw the rejections.

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Accordingly, Profit neither teaches nor suggests the limitations of independent Claim 1. Independent Claims 7, 10, 16, 21 and 25 recite limitations similar to that of independent Claim 1. Therefore, independent Claims 1, 7, 10, 16, 21 and 25 are patentable, over Profit under 35 U.S.C. 102(b), for reasons similar to that of independent Claim 1. Dependent claims are patentable by virtue of their dependency. As such, allowance of Claims 1-28 is earnestly solicited.

As per Claims 4, 9, 13, 19, 22 and 26:

Claim 4 recites a limitation whereby when the sleep function is completed, the clock is turned on and a second signal is sent to the emulator device, as claimed. Claim 4 further recites a limitation whereby the number of clock signals received at the emulator device is determined and the execution of the instructions are continued in lock-step when the determined number of clock signals equals a predetermined value, as claimed.

In comparison, Profit discloses that when clock synchronization signal is received, the RESET signal is activated causing the target bus watch circuit to release the RUN/HALT signal and allow continued execution of the target program (see Profit, col. 12, lines 24-35). Accordingly, Profit teaches that when a clock synchronization signal is received, a RESET signal is activated which as a result releases the RUN/HALT signal that allows continued execution of the target program.

CYPR-CD01208M US App. No.: 09/989,777 Art Unit: 2123 Examiner: Sharon, Ayal I "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The Applicant does not understand Profit to disclose or suggest that the number of clock signals received at the emulator device is determined, as claimed. As such, Profit neither expressly nor inherently described determining the number of clock signals received at the emulator device, as claimed.

Moreover, Profit discloses that once clock synchronization signal is received, the RESET signal is activated, releasing the RUN/HALT signal which allow continued execution of the target program. Profit fails to teach or suggest that resuming execution of the instructions are performed in lock-step, as claimed. Furthermore, Profit does not teach or suggest that execution is resumed when the number of clock signals received at the emulator device equals a predetermined value, as claimed but teaches that execution continues when RUN/HALT signal is released regardless of the number of clock signals received.

Additionally, the rejection asserts that it is inherent that the initial RUN/HALT signal "turned off" the clock. As discussed above it is not inherent that the initial RUN/HALT signal turned off the clock. In fact Profit teaches away

CYPR-CD01208M US App. No.: 09/989,777 from turning off the clock because in order to receive clock synchronization, the clock must necessarily be on. As such, the clock as disclosed by Profit has not been turned off in order to be turned on once again.

Accordingly, Profit does not teach or suggest the recited limitations of Claim 4. Claims 9, 13, 19, 22 and 26 recite limitations similar to that of Claim 4 and are patentable over Profit for reasons similar to that of Claim 4. As such, allowance of Claims 4, 9, 13, 19, 22 and 26 is earnestly solicited.

As per Claims 5 and 15:

Claim 5 recites a limitation whereby the device under test comprises a microcontroller and wherein the first signal comprises a first bit wherein the first bit received at the microcontroller indicates that a sleep function is to be performed, as claimed.

Profit on the other hand, discloses that RUN/HALT controller which resides in the communication interface halts the emulator's processor (see Profit, col. 9, line 40 to col. 10, line 31). Accordingly, Profit teaches that the controller of the communication interface, which differs from the microcontroller of the device under test, halts the emulator's processor. As such, Profit does not disclose nor does it suggest that the device under test comprises a microcontroller, as claimed. Moreover, Profit discloses that RUN/HALT controller halts the

18 CYPR-CD01208M US App. No.: 09/989,777 Examiner: Sharon, Ayal I emulator's processor whereas Claim 5 recites a limitation whereby the first bit of

the first signal received indicates that a sleep function to be performed, as

claimed. Accordingly, Profit neither expressly nor inherently described that the

device under test comprises a microcontroller and wherein the first bit of the first

signal indicates that a sleep function is to be performed, as claimed.

Accordingly, Profit does not teach or suggest the recited limitations of

Claim 5. Claim 15 recites limitations similar to that of Claim 5 and is patentable

over Profit for reasons similar to that of Claim 5. As such, allowance of Claims 5

and 15 is earnestly solicited.

As such, allowance of Claims 1-28 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and

withdrawal of rejections under 35 U.S.C. 102(b).

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CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-28 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-28 overcome the rejections of record and, therefore, allowance of Claims 1-28 is earnestly solicited.

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Respectfully submitted,

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